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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/890,471	08/01/2001	N. Edward Berg	BERG99.01CIP	3251

7590 02/13/2004

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EXAMINER

CULBERT, ROBERTS P

ART UNIT PAPER NUMBER

1763

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/890,471

Applicant(s)

BERG, N. EDWARD

Examiner

Roberts Culbert

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 18 December 2003 and 14 January 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-6,8,10,12-16,18,20,21,23,25-27,29,31 and 34-40 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6,8,10,12-16,18,20,21,23,25-27,29,31 and 34-40 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 12/18/03.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

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## **DETAILED ACTION**

### ***Response to Arguments***

Applicant's arguments filed 12/18/03 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Objections***

Claims 8, 10, 18, 23, 29, and 34-38 are objected to because of the following:

The claims depend on claims that are cancelled. Appropriate correction is required.

Claims 10, 18 and 23 are objected to because of the following: The dependent claims recite "The method of *step*..." It is clear that the claims should recite instead "The method of *claim*..." as there are no steps that correspond with the step numbers recited. Appropriate correction is required.

Claims 34 and 35 are objected to because of the following:

The term fusible is misspelled. Appropriate correction is required.

### ***Drawings***

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the step recited in claim 40 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

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Claims 35, 36, and 40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitations of claims 35 and 36 are taught in the specification (bottom of Page 7) as features that are preferable only in the conductive inks used to form the conductive layers. There is no mention of these features for printing a pattern mask as recited in Claim 31. It is not clear if the claims are intended to modify the printing of conductive inks to form the circuit patterns or the printing of pattern masks, which have a different composition.

Claim 40 is not clear because it is not stated how the first substrate is removed or what the first substrate is removed from. The specification does not provide an explanation, as it is not clear what the "beginning substrate" consists of. The beginning substrate could be the non-conducting substrate or some combination of layers including the first circuit pattern, the second circuit pattern, conductive pathways, and insulating layers. It is not clear where the separation takes place i.e. between the non-conducting substrate and the circuit pattern, or between the circuit pattern and the insulating layer. It is not stated how the stripping is performed.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-5, 12-14, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 3,660,726 to Ammon in view of U.K Patent Application Publication GB 2,227,887 A to Lowe et al.

Referring to the figures, Ammon teaches a method for making a multi-layer circuit board comprising, supplying a first substrate (10) having a first top surface and a first bottom surface; forming a plurality of electrically conductive pathways (18) between said first top surface and said first bottom

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surface; forming a first circuit pattern (16) on said first top surface; forming a second circuit pattern on said first bottom surface (19); supplying a second substrate having a second top surface and a second bottom surface; forming a plurality of electrically conductive pathways between said second top surface and said second bottom surface; forming a third circuit pattern on said second top surface; forming a fourth circuit pattern on said second bottom surface; supplying a first insulating layer (20) having a first side and a second side; joining said first side of said first insulating layer to said first bottom surface, and joining said second side of said first insulating layer to said second top surface, such that said first insulating layer electrically insulates said second circuit pattern from said third circuit pattern; forming a plurality of electrically conductive pathways (21) between said first circuit pattern, said second circuit pattern, said third circuit pattern, and said fourth circuit pattern. Ammon also shows supplying a third substrate having a third top surface and a third bottom surface; forming a plurality of electrically conductive pathways between said third top surface and said third bottom surface; forming a fifth circuit pattern on said third top surface; forming a sixth circuit pattern on said third bottom surface; supplying a second insulating layer (20) having a first side and a second side; joining said first side of said second insulating layer to said second bottom surface, and joining said second insulating layer to said third top surface, such that said second insulating layer electrically insulates said fourth circuit pattern from said fifth circuit pattern; and joining a plurality of electrically conductive pathways (21) between said first circuit pattern, said second circuit pattern, said third circuit pattern, said fourth circuit pattern, said fifth circuit pattern, and said sixth circuit pattern.

Ammon does not teach that the circuit patterns may be formed by direct printing using electro-photographic, ink jet, relief press or lithographic printing techniques.

Lowe teaches that the conductive layers, circuit devices and solder-resist masks of a circuit board may be formed by etching or by direct printing using screen-printing, transfer printing, lithographic printing or other methods. See Abstract, Examples and (Page 8, Lines 7-9), (Page 10, Lines 10-20) and (Page 18). It would have been obvious to one of ordinary skill in the art at the time of invention to use a printing technique such as lithography to form the conductive layers, circuit devices and resist masks of a circuit board since Lowe teaches that the techniques are equivalent methods of forming the conductive patterns,

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circuit devices and resist masks. Note also that since Lowe teaches that any printing method is acceptable that will handle the conducting, resistive, carbon and solder resist inks.

Claims 6, 8, 10, 15, 16, 18, 20, 21, 23, 25, 26, 27, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 3,660,726 to Ammon in view of U.K Patent Application Publication GB 2,227,887 A to Lowe et al. as applied above, and in further view of U.S. Patent 4,770,900 to Seibel.

As applied above, Ammon in view of Lowe teaches the method of the invention substantially as claimed, but does not teach the use of a semi-additive process (plating to increase thickness) to form the circuit patterns.

However, both methods of patterning the copper layer are well known in the art as alternative methods of patterning after masking. (See Seibel Col. 1, Lines 16-39)

It would have been obvious to one of ordinary skill in the art at the time of invention to either form the circuit pattern by etching or plating as both methods are notoriously old and well known in the art of circuit board formation to be suitable alternative and equivalent methods of forming a circuit pattern on a substrate.

Claims 31, 34 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,028,513 to Murakami in view of Japanese Patent Publication JP 60024990 A

Murakami teaches a prior art method of forming a circuit board, comprising steps in sequence of: supplying a non-conducting substrate having a top surface and a bottom surface each covered with a top and a bottom metallic layer, respectively; forming a pattern mask on the top and the bottom metallic layers, leaving exposed metallic patterns; building up the exposed metallic patterns by plating to increase the thickness thereof; removing the pattern mask whereby to expose the metallic patterns; and etching the metallic layer coated substrate whereby to remove exposed metallic surfaces, while leaving intact at least a portion of the built-up metallic patterns. (See, for example, Col. 1, Lines 14-16, and 30-41)

Murakami does not teach the use of printing a pattern mask on the metallic layers.

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Japanese Patent Publication 60024990 A teaches that a resist mask may be printed directly on a circuit board using lithographic printing. See Abstract. It would have been obvious to one of ordinary skill in the art at the time of invention to use lithographic printing in order to provide a high-resolution pattern as taught by the JP 60024990 A reference.

Regarding Claim 34, the mask is printed using heat-fusible ink.

Claims 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,028,513 to Murakami in view of Japanese Patent Publication JP 60024990 A and in further view of U.S. Patent 5,366,760 to Fujii et al.

As applied above, Ammon in view of Lowe teaches the method of the invention substantially as claimed, but does not teach the use of conductive ink containing a polymeric binder ink and colloidal silver or platinum.

Fujii teaches that fusible inks containing a polymeric binder resin and a colloidal metal powder such as silver is known in the art for the purpose of forming a conducting trace on a circuit board. (Col. 2, Lines 6-24) It would have been obvious to one of ordinary skill in the art at the time of invention to use fusible inks containing a polymeric binder resin and a colloidal metal powder such as silver in order to provide suitable ink for printing on a circuit board.

#### ***Allowable Subject Matter***

Claims 37 and 38 would be allowable if rewritten to overcome the claim objections set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

#### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberts Culbert whose telephone number is (571) 272-1433. The examiner can normally be reached on Monday-Friday (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory Mills can be reached on (571) 272-1439. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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